

1/10

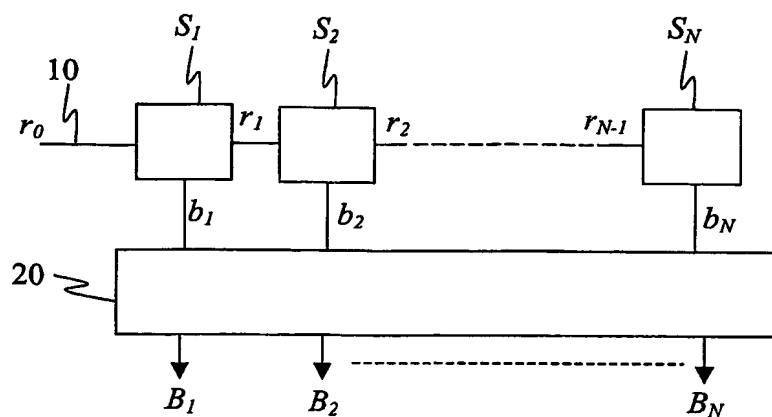


Fig. 1

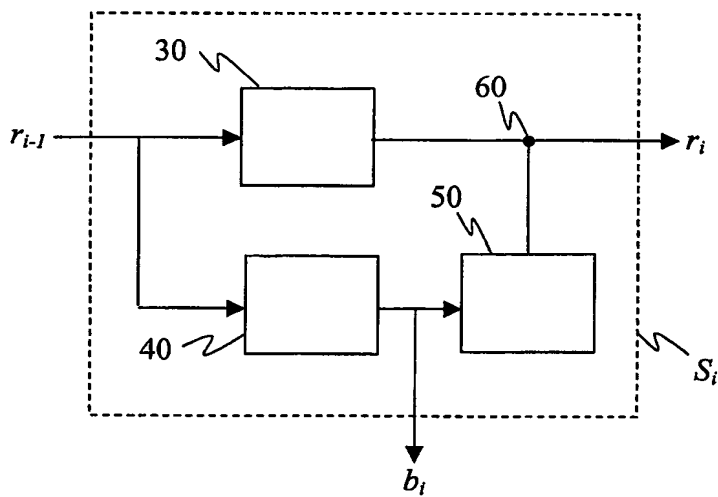


Fig. 2

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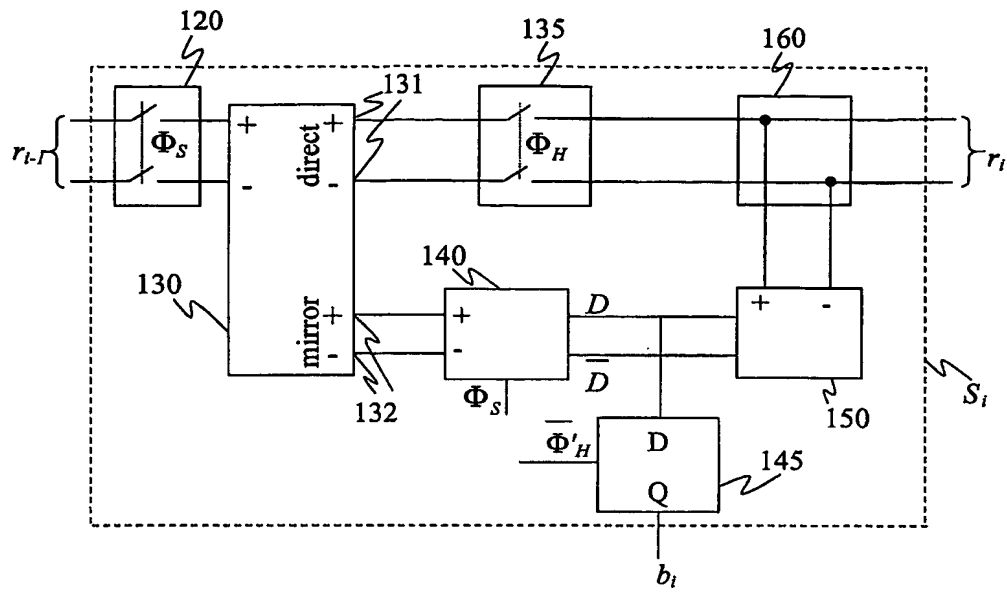


Fig. 3

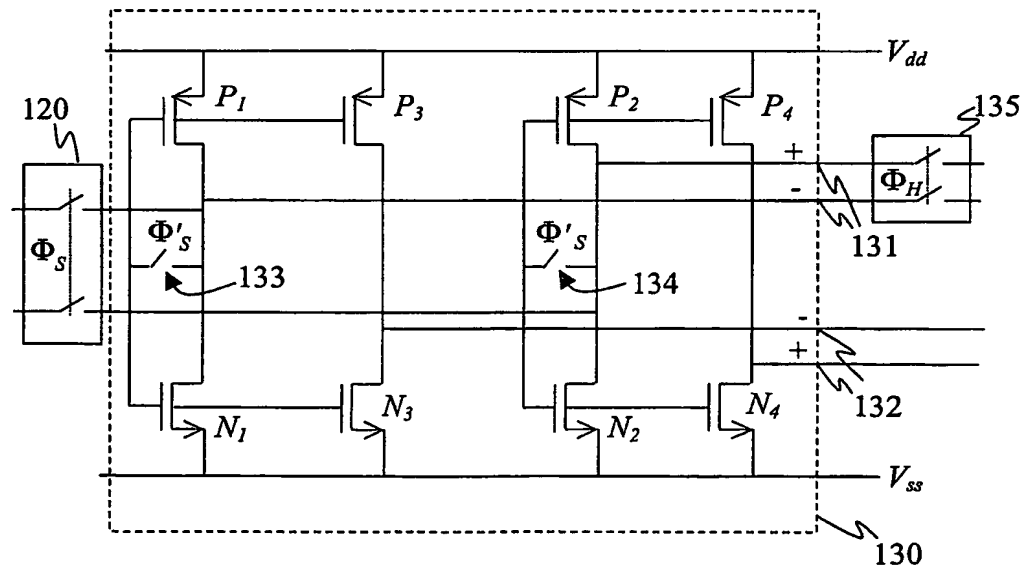


Fig. 4

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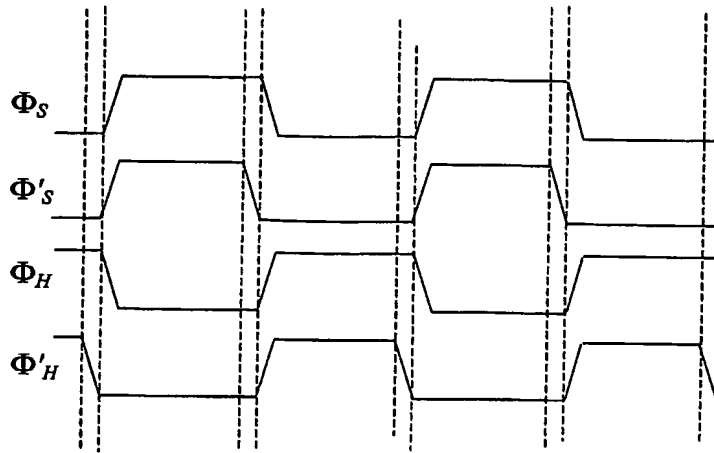


Fig. 5

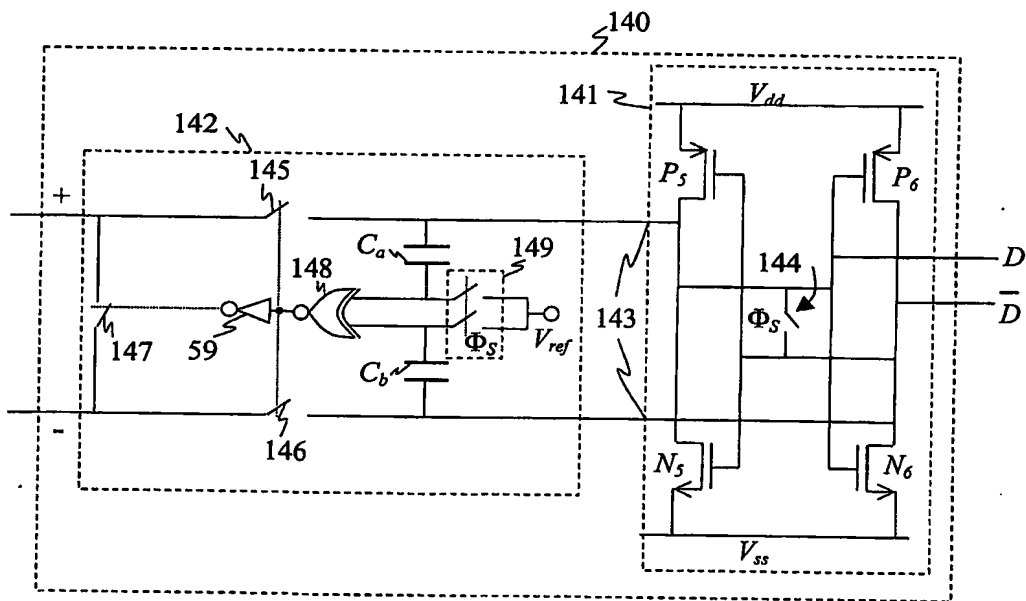
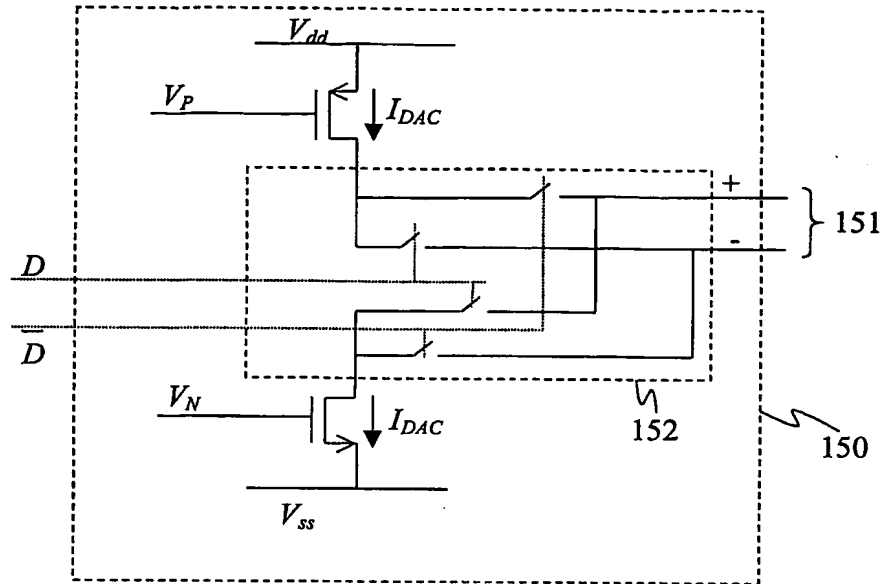
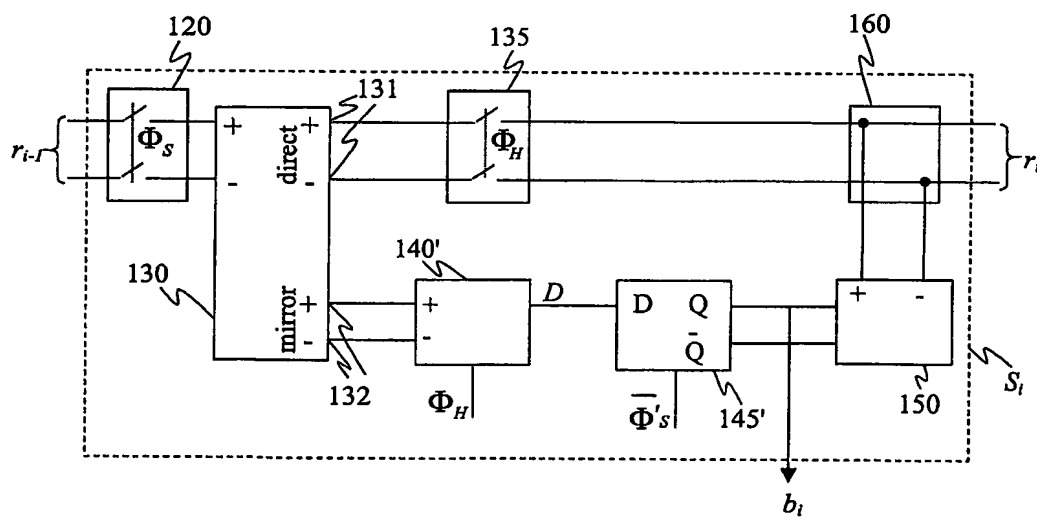


Fig. 6

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**Fig. 7**



**Fig. 8**

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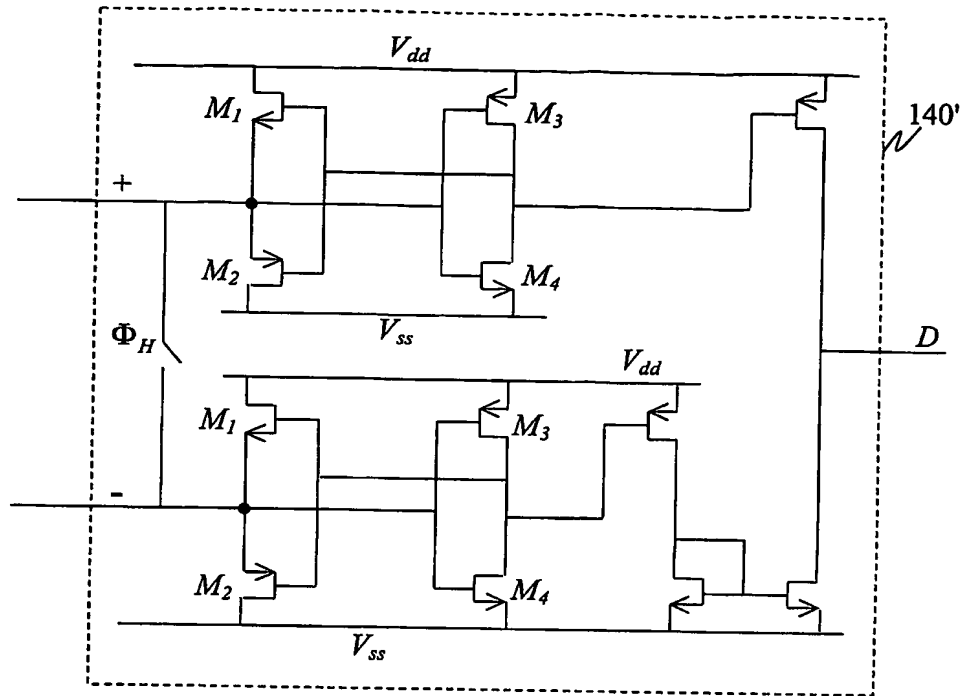


Fig. 9

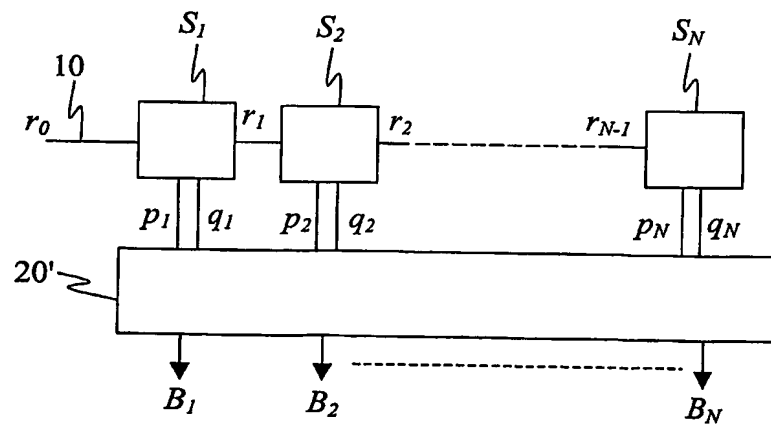


Fig. 10



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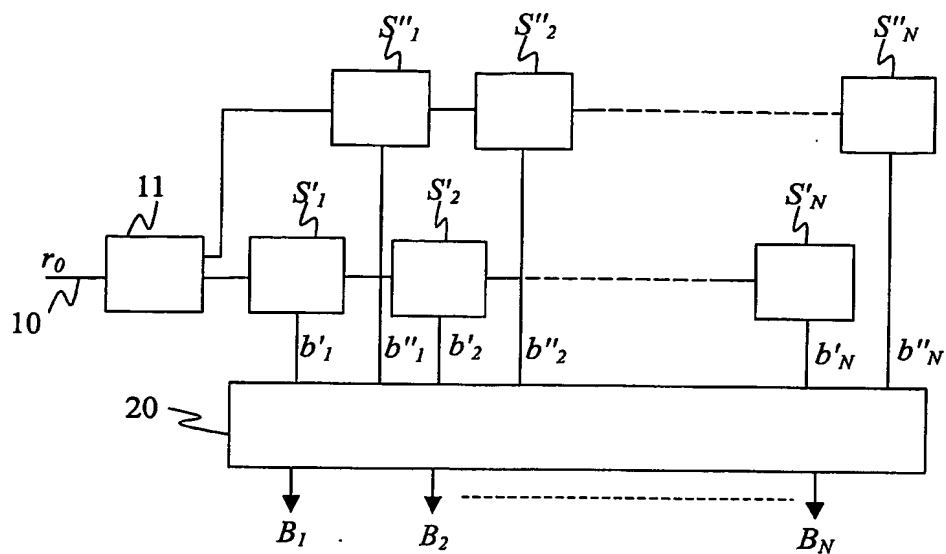


Fig. 12

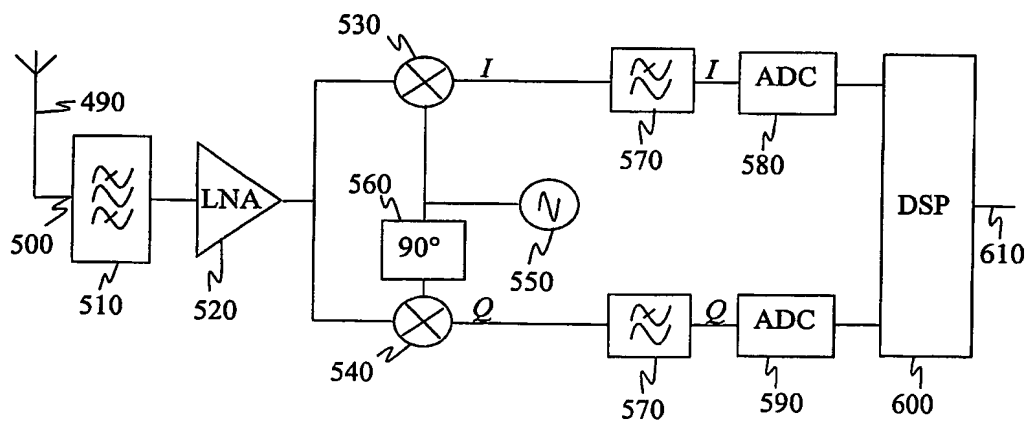


Fig. 13

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Conversion stage	Element	Clock Phase $\Phi_1$	Clock Phase $\Phi_2$
$S_i$ odd $i$	Current memory means (130)	Sampling	Holding
	Comparator means (140)	Resetting	Quantising
	DAC (150)	OFF	ON
$S_i$ even $i$	Current memory means (130)	Holding	Sampling
	Comparator means (140)	Quantising	Resetting
	DAC (150)	ON	OFF

Fig. 14

Conversion stage	Element	Clock Phase $\Phi_1$	Clock Phase $\Phi_2$
$S_i$ odd $i$	Current memory means (130)	Sampling	Holding
	Comparator means (140')	Quantising	Resetting
	DAC (150)	OFF	ON
$S_i$ even $i$	Current memory means (130)	Holding	Sampling
	Comparator means (140')	Resetting	Quantising
	DAC (150)	ON	OFF

Fig. 15

Conversion stage	Element	Clock Phase $\Phi_1$	Clock Phase $\Phi_2$
$S'_i$ , odd $i$	Current memory means (130)	Sampling	Holding
	Comparator means (140)	Resetting	Quantising
	DAC (150)	OFF	ON
$S'_i$ , even $i$	Current memory means (130)	Holding	Sampling
	Comparator means (140)	Quantising	Resetting
	DAC (150)	ON	OFF
$S''_i$ , odd $i$	Current memory means (130)	Holding	Sampling
	Comparator means (140)	Quantising	Resetting
	DAC (150)	ON	OFF
$S''_i$ , even $i$	Current memory means (130)	Sampling	Holding
	Comparator means (140)	Resetting	Quantising
	DAC (150)	OFF	ON

Fig. 16



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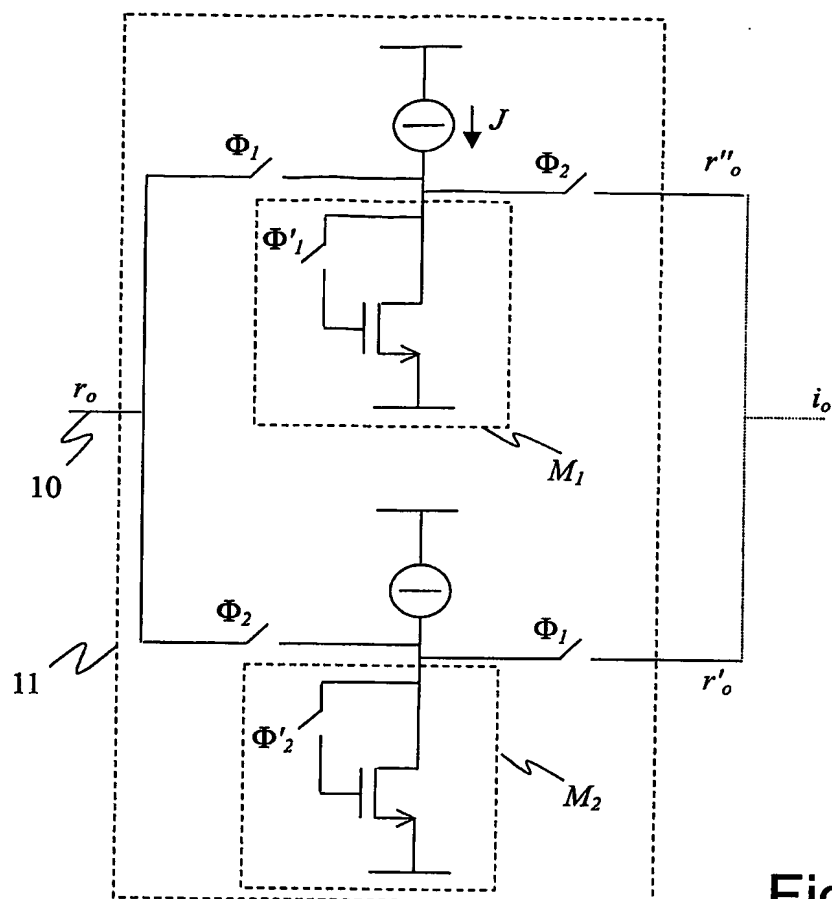


Fig. 17

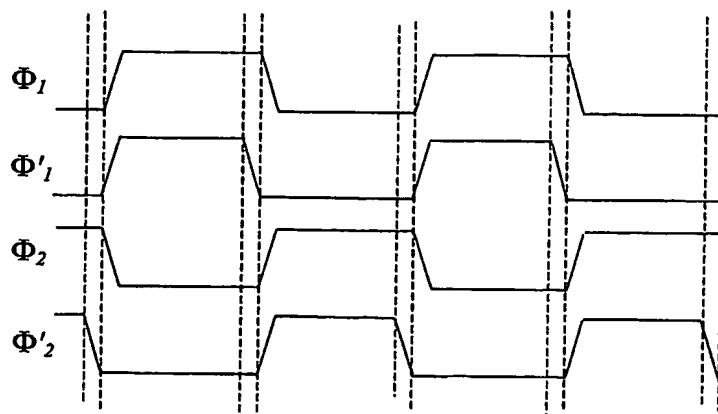


Fig. 18

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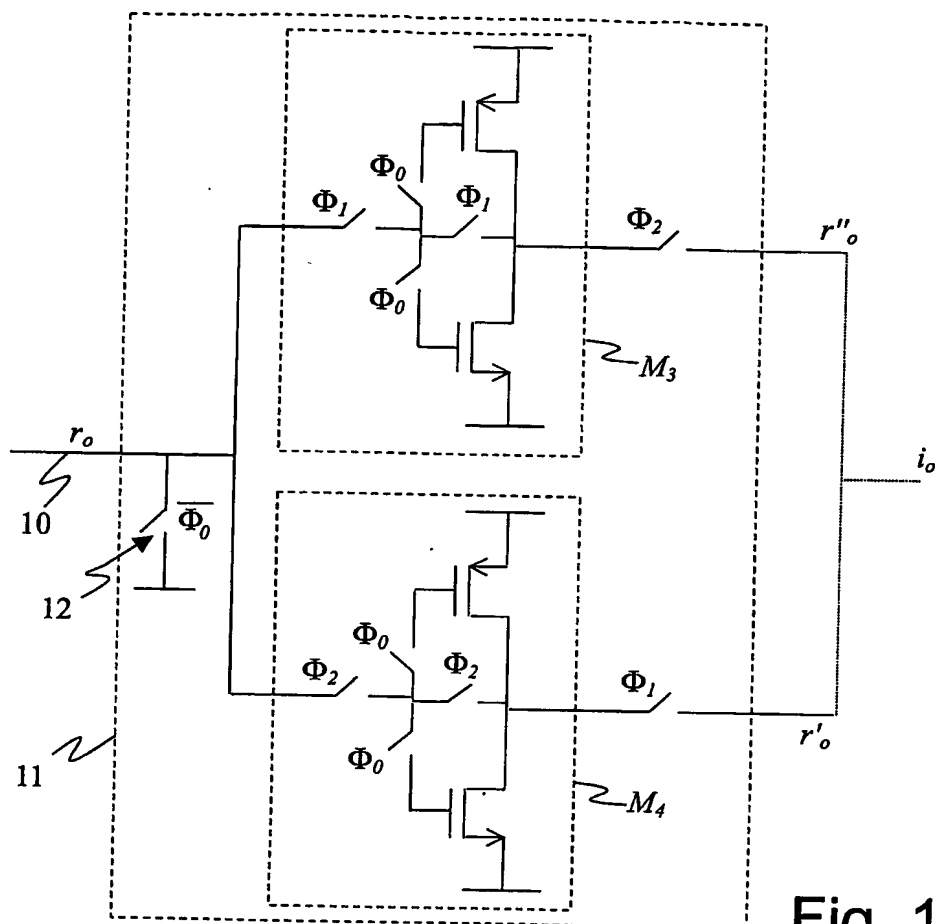


Fig. 19

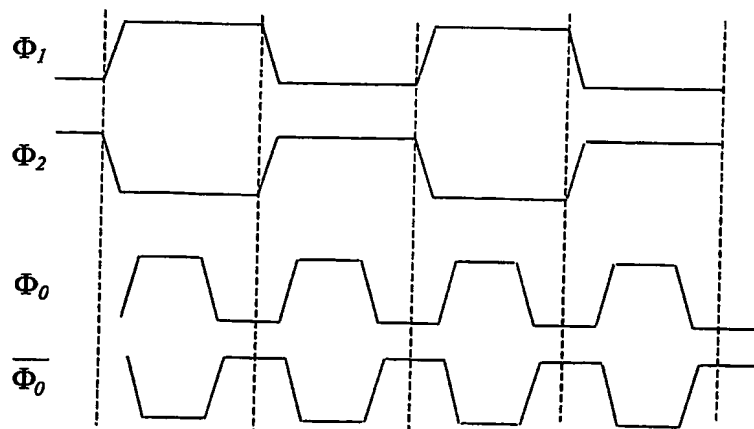


Fig. 20